REMARKS

Claims 9, 11, 12 and 16-25 are pending in the present application, were examined, and stand rejected. In response, Claims 9, 11, 12, 16-18 and 20-25 are amended. No claims are cancelled or added. Applicant respectfully requests reconsideration of pending Claims 9, 11, 12 and 16-25 in view of at least the following remarks. Reconsideration and withdrawal of the rejections of record are requested in view of such amendments and the following discussion.

I.   Claims Rejected Under 35 U.S.C. §102(e)

The Examiner has rejected Claim 23 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,477,621 issued to Lee et al. ("Lee"). Applicant respectfully traverses this rejection.

Regarding Claim 23, Claim 23 recites the following claim features, which are neither disclosed, taught nor suggested by Lee:

> at least two memory modules, each memory module including:
> at least one bank of memory devices, and
> a memory module buffer, having a data cache coupled to an eviction buffer, both coupled to the bank of memory devices, the memory module buffer including a command deserializer and decoder unit to control the data cache and the eviction buffer according to a plurality of commands delivered by a memory controller, the commands sequentially delivered over a plurality of transfer periods of a memory access transaction, the plurality of commands including an activate command and a writeback command, the eviction buffer to store one or more lines of data evicted from the data cache. (Emphasis added.)

Apposite to amended Claim 23, cache row address registers 701-707, as shown in Fig. 3 of Lee, neither disclose, teach nor suggest the eviction buffer to store one or more lines of data evicted from the data cache, let alone the memory module buffer including a command deserializer and decoder unit to control the data cache and eviction buffer according to a plurality of commands sequentially delivered over a plurality of transfer periods of a memory access transaction, as in Claim 23. As disclosed by Lee:

> Each of channel row cache memories 601-607 is associated with a corresponding one of cache row address registers 701-707. Each of cache row address registers 701-707 stores N cache addresses. That is, each cache entry in channel row cache memories 601-607 has a corresponding cache address stored in

a corresponding one of <u>cache row address registers</u> 701-707. (Col. 8, lines 41-47.)

Furthermore, the Examiner relies on cache row address registers 701-707 to disclose the eviction buffer recited by Claim 23. However, as explicitly disclosed by <u>Lee</u>, the cache row address registers 701-707 store N cache addresses. (See col. 8, lines 41-44.) As disclosed by <u>Lee</u>, each cache entry in channel row cache memory 601-607 has a corresponding cache address stored in a corresponding one of the cache row address registers 701-707. (See col. 8, lines 44-47.) Consequently, since <u>Lee</u> teaches that cache row address registers 701-707 are used to store a cache address corresponding to each cache entry within channel row cache memory 601-607, the cache row address registers 701-707, as shown in FIG. 3 of <u>Lee</u>, can neither disclose, teach nor suggest the eviction buffer to store one or more lines of data evicted from the data cache, as in Claim 23.

Therefore, for at least the reasons provided above, Claim 23 is patentable over <u>Lee</u>, as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(b) rejection of Claim 23.

II.   Claims Rejected Under 35 U.S.C. §103(a)

The Examiner has rejected Claims 20-22 and 24-25 under 35 U.S.C. §103(a) as being unpatentable over <u>Lee</u> in view of U.S. Patent No. 5,526,510 issued to Akkary et al. ("<u>Akkary</u>"). Applicant respectfully traverses this rejection.

Regarding Claim 20, Claim 20 recites a memory module, which includes the following claim features, which are neither taught nor suggested by the combination of <u>Lee</u> in view of <u>Akkary</u>:

> at least one bank of <u>memory devices</u>; and
> a memory module buffer having a <u>data cache</u> coupled to an <u>eviction buffer</u>, both coupled to the bank of memory devices, the memory module buffer including <u>a command deserializer and decoder unit</u> to <u>control</u> the <u>data cache</u> and the <u>eviction buffer</u> according to a plurality of <u>commands delivered</u> by a memory controller over a memory bus, the commands <u>sequentially delivered</u> over a <u>plurality of transfer periods</u> of a memory access transaction, the plurality of commands including an <u>activate command</u> and a <u>writeback command</u>,
> the <u>command deserializer and decoder unit</u> to receive a <u>writeback command</u>, the command deserializer and decoder unit to <u>cause a previous line</u> of

data, evicted from the data cache and stored within the eviction buffer, to be written out of the eviction buffer to the bank of memory devices. (Emphasis added.)

As indicated above with regard to the §102(b) rejection of Claim 23, since cache row address registers 701-707 do not store previous data evicted from the channel row cache memories 601-607, Lee cannot teach that evicted data is stored within cache row address registers 707 nor that such evicted data is written out of the registers 701-707 to the memory banks 301-304, as recited by Claim 20. Furthermore, Lee does not disclose, teach or suggest a memory module buffer including a command deserializer and decoder unit to control the data cache and the eviction buffer according to a plurality of commands delivered by a memory controller over a memory bus, as in Claim 20.

Regarding the Examiner's citing of Akkary, assuming, arguendo, that Akkary teaches the features performed by the command deserializer and decoder unit in response to a writeback command, as recited by Claim 20, modifying of Lee to write the cache addresses stored within cache row address registers 701-707 to memory banks 301-304, as recited by Claim 23, results in the addresses stored within address registers 701-707 being written out of registers 701-707 to memory banks 301-304. However, for at least the reasons indicated above, memory banks 301-304, as taught by Lee, are used to store data, and not the addresses corresponding to such data.

In contrast to Claim 20, Lee fails to teach or suggest a memory module buffer including a command deserializer and decoder unit to control the data cache and the eviction buffer according to a plurality of commands delivered by a memory controller over a memory bus, let alone that the commands are sequentially delivered over a plurality of transfer periods of a memory access transaction, as recited by Claim 20. Furthermore, the Examiner's citing of Akkary fails to rectify the failure of Lee to disclose, teach or suggest that the plurality of commands include an activate command and a writeback command, as recited by Claim 20.

For at least the reasons indicated above, since the cache row address registers 701-707, as taught by Lee, neither teach nor suggest an eviction buffer, as recited by Claim 20, one skilled in the art would not modify, and could not modify Lee, as taught by Akkary, to write data addresses from registers 701-707 to the memory banks 301-304 (see FIG. 3 and 5 of Lee) since storage of such addresses could result in the loss of data from channel row cache memories 601-607.

Accordingly, Applicant respectfully submits that the combined teachings of Lee in view of Akkary would not have suggested the claimed subject matter to one of ordinary skill in the art.

Consequently, Applicant respectfully submits that the prior art combination of Lee in view of Akkary fail to teach or suggest all claim features recited by Claim 20, as required to establish *prima facie* obviousness.

Therefore, Applicant respectfully submits that Claim 20 as well as Claims 21 and 22, based on their dependency from Claim 20, are patentable over the combination of Lee in view of Akkary. Id. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 20, 21 and 22.

Regarding Claims 24 and 25, Claims 24 and 25, based on their dependency from Claim 23, would also be patentable over the combination of Lee in view of Akkary, since Akkary fails to teach or suggest a memory module buffer including a command deserializer and decoder unit to control the data cache and the eviction buffer according to a plurality of commands delivered by a memory controller, as in Claim 23. Therefore, for at least the reasons provided above, Applicant respectfully submits that Claims 24 and 25, based on their dependency from Claim 23, are also patentable over the combination of Lee in view of Akkary. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 24 and 25.

The Examiner has rejected Claims 9, 11-12 and 16-19 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,378,049 issued to Stracovsky et al. ("Stracovsky") in view of Lee and Akkary. Applicant respectfully traverses this rejection.

Regarding Claim 9, Claim 9 recites a memory module including the following features, which are neither disclosed, taught nor suggested by the combination of Stracovsky in view of Lee and further in view of Akkary:

> at least one bank of memory devices, and
> a memory module buffer having a data cache coupled to an eviction buffer, both coupled to the bank of memory devices, the memory module buffer including a command deserializer and decoder unit to control the data cache and the eviction buffer according to a plurality of commands delivered by the memory controller, the commands sequentially delivered over a plurality of transfer

periods of a memory access transaction, the plurality of commands including an activate command and a writeback command, the memory controller to issue a write transaction, the command deserializer and decoder unit to store a current line of data within the data cache until the memory controller signals the command deserializer and decoder unit an eviction to instruct the data cache to evict the current cache line of data from the data cache into the eviction buffer. (Emphasis added.)

Applicant respectfully submits that the above-recited features of Claim 9 are analogous to the above-recited features of Claim 20. Accordingly, Applicant's arguments provided above with regard to the §103(a) rejection of Claim 20 apply to the Examiner's §103(a) rejection of Claim 9.

Moreover, the Examiner's citing of Stracovsky fails to rectify the failure of Lee in view of Akkray to teach or suggest a memory module buffer including a command deserializer and decoder unit to control the data cache and the eviction buffer according to a plurality of commands delivered by a memory controller over a memory bus, as recited by Claim 9.

Consequently, Applicant respectfully submits that the combination of Stracovsky in view of Lee and further in view of Akkary, cannot teach all claim features recited by Claim 9, as required to establish a *prima facie* case of obviousness. Id. Therefore, for at least the reasons provided above, Applicant respectfully submits that Claim 9 is patentable over the prior art combination of Stracovsky in view of Lee and further in view of Akkary.

Hence, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 9, as well as the §103(a) rejection of Claims 11-12, which based on their dependency from Claim 9, are also patentable over the combination of Stracovsky in view of Lee and further in view of Akkary.

Regarding Claim 16, Claim 16 recites the following claim features, which are neither disclosed nor suggested by the combination of Stracovsky in view of Akkary:

> an array of tag address storage locations; and
> a command sequencer and serializer unit coupled to the array of tag
> address storage locations, the command sequencer and serializer unit to control a
> data cache and an eviction buffer located on a memory module buffer of at least
> one memory module of a system memory, the commands sequentially delivered
> over a plurality of transfer periods of a memory access transaction, the plurality of
> commands including an activate command and a writeback command, the

command sequencer and serializer to <u>deliver</u> a <u>writeback command</u> to the <u>eviction buffer</u> associated with the memory module, the writeback command to <u>cause</u> a <u>previous line of data evicted</u> from the <u>data cache</u> and <u>stored</u> in the <u>eviction buffer</u>, to be <u>written out</u> to <u>a memory device</u> of the memory module. (Emphasis added.)

Applicant respectfully submits that the above-recited features of Claim 16 are analogous to the above-recited features of Claim 9. Accordingly, Applicant's arguments provided above with regard to the §103(a) rejection of Claim 9 apply to the Examiner's §103(a) rejection of Claim 16.

Hence, for at least the reasons indicated above, the combination of <u>Stracovsky</u>, <u>Lee</u> and <u>Akkray</u> does not teach or suggest a command sequencer and serializer unit to control a data cache and an eviction buffer located on a memory module buffer of at least one memory module of a system memory recited by Claim 16.

Consequently, Applicant respectfully submits that the prior art combination of <u>Stracovsky</u> in view of <u>Lee</u> and further in view of <u>Akkary</u>, fails to at least teach or suggest a data cache and an eviction buffer located on at least one memory module of the system memory, as recited by Claim 16. Hence, Applicant respectfully submits that Claim 16 is patentable over the combination of <u>Stracovsky</u> in view of <u>Akkary</u>. <u>Id</u>. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 16.

Regarding Claims 17-19, Claims 17-19, based on their dependency from Claim 16, are also patentable over the prior art combination of <u>Stracovsky</u> in view of <u>Akkary</u>. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 17-19.
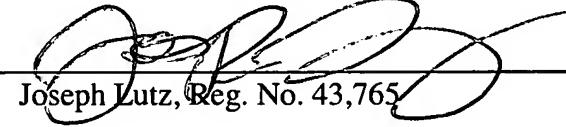
CONCLUSION

In view of the foregoing, it is submitted that Claims 9, 11, 12 and 16-25 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

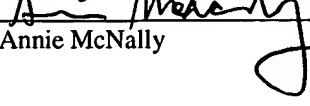BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

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